I claim:

1. A test architecture within an integrated circuit comprising;

A. a plurality of core wrappers each free of 1149.1 test access ports and each having a serial input, a serial output, and control inputs,

B. input circuitry having a serial input, a plurality of serial outputs, and control inputs,

C. output circuitry having a plurality of serial inputs, a serial output, and control inputs,

D. first connections formed between ones of said plurality of serial outputs and ones of said serial inputs of said plurality of core wrappers, and

E. second connections formed between ones of said serial outputs of said plurality of core wrappers and ones of said plurality of serial inputs.

2. The test architecture of claim 1 further including third connections between said control inputs of said core wrappers.

3. A plurality of test architectures of claim 1 arranged in parallel between further input circuitry and further output circuitry, the serial inputs to the input circuitry of said plurality of test architectures being connected to outputs from said further input circuitry and the serial outputs from the output circuitry of said plurality of test architectures being connected to inputs to said further output circuitry.

4. A plurality of test architectures of claim 1 connected in a serial arrangement, the serial output of the output circuitry of one test architecture being connected to serial input of the input circuitry of another test architecture.

5. A plurality of test architectures of claim 1 connected in a serial arrangement, the serial output of the output circuitry of one test architecture being coupled to serial input of the input circuitry of another test architecture through a circuit.

6. Test circuitry within an integrated circuit comprising;

A. a plurality of core wrappers each free of 1149.1 test access ports and each having a serial input, a serial output, and control inputs,

B. output circuitry having inputs connected to the serial outputs of said core wrappers and having an output, and

C. a shift register having an input connected to the output of said output circuitry.

7. A process of communicating serial data through first and second core wrapper arrangements within an integrated circuit comprising:

A. performing a first serial data communication through a first core wrapper arrangement and a shift register external of said first core wrapper arrangement, and

B. performing a second serial data communication through a second core wrapper arrangement and a shift register external of said second core wrapper arrangement.

8. A process of enabling access to a lower test architecture embedded within a higher test architecture comprising:

A. performing a first scan operation to load a first code into a register of said higher test architecture; and

B. performing a second scan operation to reload said first code into the register of said higher test architecture and to load a second code into a register of said lower test architecture.

9. An electronic system comprising;

A. a plurality of circuits each having an input and an output,

B. a data path formed between the output of a first of said plurality of circuits and the input of a second of said plurality of circuits, and

C. circuitry within the data path selectively operating in one of a first mode to register the data from said output to said input and a second mode to directly pass the data from said serial output to said serial input.